sense nodes for [imperfectly isolating] receiving an enabling voltage for causing current leakage therethrough between said sense nodes [from] and the bit line while maintaining high resistance [whereby current can leak therethrough],

(e) means for enabling said sense amplifier and establishing full predetermined logic levels across said sense nodes,

(f) means for disabling said imperfect isolating means and thereby removing [said] isolation between said sense nodes and the bit line,

whereby current passing through the sense amplifier to said sense nodes is enabled to charge said bit line capacitance through said imperfect isolating means to a predetermined logic voltage level.

Claim 2, line 2, prior to "isolating" insert --imperfect--.

3. (Amended) A DRAM as defined in claim [1 in which said means for disabling is comprised of] 2 including a voltage source applied to gates of each field effect transistor having an initial voltage level which is higher than said logic voltage level and a following enabling voltage level which is equal to said logic level, and at a later time a disabling voltage equal to the initial voltage level.

5. (Amended) A DRAM as defined in claim [1 in which said means for disabling is comprised of] 4 including

a voltage source applied to gates of each field effect transistor having an initial voltage level which is lower than said logic voltage level and a following enabling voltage level which is equal to said logic level, and at a later time a disabling voltage equal to said initial voltage level.

6. (Amended) A dynamic random access memory (DRAM) comprising:

(a) a plurality of bit storage capacitors,

(b) a folded bit line for receiving charge stored on one of said capacitors having bit line capacitance,

(c) a sense amplifier having a pair of sense nodes for sensing a voltage differential across said sense nodes, the sense amplifier having respective sense enable and restore enable inputs for providing full high and full low logic levels respectively to said sense nodes,

(d) power supply means for providing full high and full low logic level voltages,

(e) a pair of field effect transistors, one being a P-channel enhancement mode type having its source-drain circuit connected between said restore enable input and the high logic level power supply voltage and the other being an N-channel enhancement mode type having its source-drain circuit connected between the sense enable input and the low logic level power supply voltage, and